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APPLICATION FOR LETTERS PATENT

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METHOD IN AN INTEGRATED CIRCUIT (IC) MANUFACTURING PROCESS FOR IDENTIFYING AND REDIRECTING IC'S MIS-PROCESSED DURING THEIR MANUFACTURE

Inventor:
Raymond J. Beffa

Attorney:
James R. Duzan
Registration No. 28,393
TRASKBRITT, PC
P.O. Box 2550
Salt Lake City, Utah 84110
(801) 532-1922

TITLE OF THE INVENTION

METHOD IN AN INTEGRATED CIRCUIT (IC) MANUFACTURING PROCESS FOR IDENTIFYING AND REDIRECTING IC'S MIS-PROCESSED DURING THEIR MANUFACTURE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of application Serial No. 10/067,728, filed February 4, 2002, pending, which is a continuation of application Serial No. 09/793,938, filed February 27, 2001, now U.S. Patent 6,363,329 B2, issued March 26, 2002, which is a continuation of application Serial No. 09/537,839, filed March 29, 2000, now U.S. Patent 6,208,947 B1, issued March 27, 2001, which is a continuation of application Serial No. 09/302,338, filed April 29, 1999, now U.S. Patent 6,067,507, issued May 23, 2000, which is a continuation of application Serial No. 08/806,442, filed February 26, 1997, now U.S. Patent 5,915,231, issued June 22, 1999, which is related to: co-pending Serial No. 08/591,238, filed January 17, 1996, now abandoned; Serial No. 08/664,109, filed June 13, 1996, now U.S. Patent 5,895,962, issued April 20, 1999; and Serial No. 08/785,353, filed January 17, 1997 now U.S. Patent 5,927,512, issued July 27, 1999.

BACKGROUND OF THE INVENTION

[0002] Field of the Invention: The present invention relates in general to integrated circuit (IC) manufacturing and, more specifically, to methods in IC manufacturing processes for identifying and redirecting IC's mis-processed during their manufacture.

[0003] State of the Art: As shown in FIG. 1, a typical process 10 for manufacturing very small electronic circuits referred to as "Integrated Circuits" (IC's) begins with the IC's being formed or "fabricated" on the surface of a wafer 12 of semiconductor material, such as silicon. Once fabricated, IC's are electronically probed to determine whether they are functional (i.e., "good") or nonfunctional (i.e., "bad"), and a computer then stores an electronic wafer map 14 of the wafer 12 identifying the locations of the good and bad IC's on the wafer 12.

[0004] After being probed, IC's are sawed from their wafer 12 into discrete IC dice or "chips" using high-speed precision dicing equipment. IC dice identified as good by their wafer map 14 are then each "picked" by automated equipment from their sawed wafer 12 and "placed" on an epoxy coated bonding site of a lead frame, while IC dice identified as bad are discarded into a scrap bin 16. The epoxy attaching the good IC dice to their lead frames is then allowed to cure, and the attached dice are wire bonded to their lead frames using high speed bonding equipment. At this point in the process 10, the lead frames of IC dice are still connected to other lead frames.

[0005] Once wire bonded, IC dice and their lead frames are formed into IC packages using a hot thermosetting plastic encapsulant injected into a mold. Leads of the lead frames project from the IC packages after encapsulation, and these leads are dipped in a cleansing chemical bath in a process referred to as "de-flash." After de-flash, IC packages are cured to set their plastic encapsulant, and their projecting leads are then electroplated with a lead/tin finish.

[0006] After lead finishing, connections between the lead frames of different IC packages are cut to "singulate" the IC packages into discrete IC devices. Discrete devices are then tested in a simple electronic test that checks for "opens" (i.e., no connection) within the devices where connections should exist and "shorts" (i.e., a connection) where connections should not exist. Devices that fail the opens/shorts test are discarded into the scrap bin 16, and devices that pass proceed to extensive back-end test procedures where they are tested for functionality and operability before being shipped to customers.

[0007] On occasion, bad IC dice are accidentally picked from a sawed wafer 12 for subsequent assembly and back-end testing as described above. This can happen, for example, because a human, software, or electronic error causes the automated pick and place equipment described above to access the wrong wafer map 14 for a wafer 12. It can also happen because of a misalignment, referred to as a "registration" error, between the automated pick and place equipment and a wafer 12. In either case, such accidents typically are not detected until the bad IC dice undergo at least some back-end testing and, as a result, waste back-end testing resources. Therefore, there is a need in the art for a method of identifying and discarding accidentally assembled IC dice before the dice undergo back-end testing procedures.

[0008] As described in U.S. Patent No.'s 5,301,143, 5,294,812, and 5,103,166, some methods have been devised to electronically identify IC dice. Such methods take place "off" the manufacturing line, and involve the use of electrically retrievable identification (ID) codes, such as so-called "fuse ID's," programmed into individual IC dice to identify the dice. The programming of a fuse ID typically involves selectively blowing an arrangement of fuses or anti-fuses in an IC die so that when the fuses or anti-fuses are accessed, they output a selected ID code. Unfortunately, none of these methods addresses the problem of identifying and discarding accidentally assembled IC dice "on" a manufacturing line.

BRIEF SUMMARY OF THE INVENTION

[0009] The present invention provides a method that can identify and discard accidentally assembled integrated circuit (IC) dice "on" an IC manufacturing line before the dice undergo back-end testing procedures.

[0010] In one embodiment, the method identifies and redirects IC's that have been mis-processed, such as bad IC's identified at probe that have accidentally been assembled and packaged. The method includes storing data, such as an electronic wafer map, at probe, for example, in association with a unique identification (ID) code, such as a fuse ID, of each of the IC's. The stored data indicates a process flow within the IC manufacturing process that each of the IC's should undergo. For example, the stored data may indicate that an IC is bad and should be discarded, or that an IC is good and should be assembled and packaged.

[0011] As described above, on occasion, one or more IC's do not undergo the process flow they should undergo. For example, some bad IC's may proceed through assembly and packaging rather than being discarded. To check for IC's that have not undergone the process flow they should undergo, the present method also includes reading the ID code of each of the IC's at, for example, the opens/shorts test at the end of assembly. The data (e.g., the wafer map) stored in association with the ID code of each of the IC's is then accessed and evaluated to identify any IC's that have undergone a process flow within the IC manufacturing process that is different from the process flow their data indicates they should have undergone, such as bad IC's that have proceeded through assembly and packaging. Any IC's identified as having been mis-

processed are then redirected within the IC manufacturing process. Thus, for example, bad IC's that have been assembled and packaged may be discarded so they do not proceed to back-end testing.

[0012] In another embodiment of the present invention, a method of manufacturing IC devices, such as Dynamic Random Access Memory Devices (DRAM's), from semiconductor wafers includes providing the semiconductor wafers and fabricating IC's on the wafers. A substantially unique ID code, such as a fuse ID, is then stored in each of the IC's, and data is stored in association with the ID code of each of the IC's that indicates a manufacturing process flow that each of the IC's should undergo. Each IC is then separated from its wafer to form an IC die, and the IC dice are assembled into IC devices, such as wire bond/lead frame devices, Chip On Board (COB) devices, or flip-chip devices. The ID code associated with each of the IC devices is then read, and the data stored in association with the ID code associated with each of the IC devices is accessed and evaluated to identify any IC devices that have undergone a manufacturing process flow that is different from the manufacturing process flow their data indicates they should have undergone. These identified IC devices are then redirected (e.g., discarded), and the remaining IC devices continue on to back-end testing.

[0013] A further embodiment of the present invention comprises a method of manufacturing Multi-Chip Modules (MCM's) similar to the method of manufacturing IC devices described above.

[0014] A still further embodiment of the present invention comprises another method of manufacturing IC devices from semiconductor wafers. The method includes providing the semiconductor wafers and fabricating IC's on the wafers. Each IC is electronically probed to identify good and bad IC's on the wafers and then programmed with a unique fuse ID. An electronic wafer map is stored for each wafer indicating the locations of good and bad IC's on the wafer and associating each IC on the wafer with its fuse ID. Each IC is then sawed from its wafer to form a discrete IC die that is automatically picked and placed on an epoxy coated bonding site of a lead frame. The epoxy is allowed to cure, and the IC dice are then wire bonded to their respective lead frames. Next, the IC dice and their associated lead frames are injection molded to form IC packages. Projecting leads of the packages are then de-flashed, the packages

are cured, and the leads are then electroplated. Then, each package is singulated to form a discrete IC device, and each device is tested for opens and shorts. The fuse ID associated with each IC device is then electrically retrieved so the wafer map stored in association with the fuse ID associated with each of the IC devices may be accessed and evaluated to identify any IC devices that include a bad IC and any IC devices that include a good IC. Any IC devices identified as including a bad IC are discarded, and any IC devices identified as including a good IC proceed to back-end testing.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0015] FIG. 1 is a flow diagram illustrating a conventional integrated circuit (IC) manufacturing process; and

[0016] FIG. 2 is a flow diagram illustrating an IC manufacturing process in which accidentally assembled IC dice are identified and discarded in accordance with the present invention before back-end testing.

DETAILED DESCRIPTION OF THE INVENTION

[0017] As shown in FIG. 2, an inventive method 20 for manufacturing integrated circuits (IC's) from a group of semiconductor wafers 22 includes the step 24 of fabricating the IC's on the wafers 22. It will be understood by those having skill in the field of this invention that the present invention is applicable to any IC devices, including Dynamic Random Access Memory (DRAM) IC's, Static Random Access Memory (SRAM) IC's, Synchronous DRAM (SDRAM) IC's, processor IC's, Single In-line Memory Modules (SIMM's), Dual In-line Memory Modules (DIMM's), and other Multi-Chip Modules (MCM's). It will also be understood that although the present invention will be described below in the context of a wire bond/lead frame assembly process, the present invention is applicable to any IC assembly process, including, for example, Chip On Board (COB), flip chip, and Tape-Automated Bonding (TAB) processes.

[0018] After fabrication, the IC's are electronically probed in a probe step 28 to evaluate a variety of their electronic characteristics, and data from the probe step 28 identifying bad and good IC's are noted and stored as wafer maps 30, as described above. During the probe

step 28, IC's fabricated on the wafers 22 are programmed in the manner described above with a fuse identification (ID) unique to each IC. The fuse ID for each IC is then stored in association with the wafer maps 30 such that each die location on each wafer map 30 is associated with the unique fuse ID of a particular IC. The fuse ID may identify, for example, a wafer lot ID, the week the IC's were fabricated, a wafer ID, a die location on the wafer, and a fabrication facility ID.

[0019] It will be understood, of course, that the present invention includes within its scope IC's having any ID code, including those having fuse ID's. It will also be understood that the IC's may be programmed with their fuse ID's at steps in the manufacturing process 20 other than the probe step 28.

[0020] Once programmed, the IC's proceed through an assembly process 32 to an opens/shorts test 34 as described above. At the opens/shorts test 34, the fuse ID of each IC is automatically read and correlated with the wafer map 30 of its wafer 22. If a bad IC has accidentally proceeded through the assembly process 32, the fuse ID of the IC, in correlation with the wafer map 30 of the IC's wafer 22, will identify the IC as a bad IC so it can be discarded to a scrap bin 36 instead of proceeding through back-end testing. The present invention thus provides a method of identifying and discarding accidentally assembled IC's before they undergo back-end testing.

[0021] It should be understood that although the fuse ID's of IC's in the process 20 are typically read electronically, they may also be read optically if the fuse ID's consist of "blown" laser fuses that are optically accessible. It should also be understood that the present invention includes within its scope any method in an IC manufacturing process for identifying and redirecting IC's mis-processed during their manufacture using ID codes such as fuse ID's.

[0022] Although the present invention has been described with reference to a preferred embodiment, the invention is not limited to this embodiment. For example, while the various steps of the preferred embodiment have been described as occurring in a particular order, it will be understood that these steps need not necessarily occur in the described order to fall within the scope of the present invention. Thus, the invention is limited only by the appended claims,

which include within their scope all equivalent methods that operate according to the principles of the invention as described.